Low-Voltage Low-Power CMOS-RF Transceiver Design

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Invited Paper

***Abstract*—Research over the last ten years has resulted in attempts toward single-chip CMOS RF circuits for Bluetooth, global positioning system, digital enhanced cordless telecommunications and cellular applications. An overview of the use of CMOS for low-cost integration of a high-end cellular RF transceiver front-end is presented. Some fundamental pitfalls and limitations of RF CMOS are discussed. To circumvent these obstacles, the choice of transceiver architecture, circuit topology design, and systematic optimization of the different transceiver blocks is necessary. Moreover, optimization of the transceiver as one single block by minimizing the number of power-hungry interface circuits is emphasized. As examples, a fully integrated cellular transceiver front-end, a low-power extremely low noise-figure low-noise amplifier, and a very efficient power amplifier are demonstrated.**

***Index Terms*—CMOS, low power, low voltage, receiver, RF, transceiver, wireless.**

I. Introduction

THE end of the 20th Century will be remembered for the unrivaled growth of the telecommunication industry. The main cause for this event was the introduction of digital signal processing in wireless communications, driven by the development of high-performance low-cost CMOS technologies for very large scale integration (VLSI). However, the RF analog front-end remains the bottleneck for low-cost RF systems. RF front-end design is pushed toward higher levels of integration and integration in cheap CMOS technology, rendering significant space, cost and power reductions. The ultimate goal is full integration: both the analog front-end and the digital demodulator being on the same die. Since front-ends have to detect very weak (f_W's) high-frequency (HF) signals and have to transmit HF high-power levels (up to 2 W), high-performance analog circuits are required. The advantages of deep submicrometer CMOS technologies is that the f_T's of the NMOS devices are getting close to the f_T's of the n-p-n devices. In this paper, an overview is presented in order to demonstrate the suitability of standard CMOS for the integration of high-quality low-power RF transceiver front-ends without exotic technology adaptations [1]. Several circuit examples will be presented in the area of global positioning system (GPS) receiver (RX) and cellular transceivers. A fully integrated CMOS cellular transceiver front-end achieves DCS-1800 class I/II specifications and features a high level of integration. To build a complete transceiver system, only an antenna, an antenna filter, a power amplifier, a crystal oscillator, and a digital baseband (BB) chip must be added to the analog front-end (see Fig. 1).

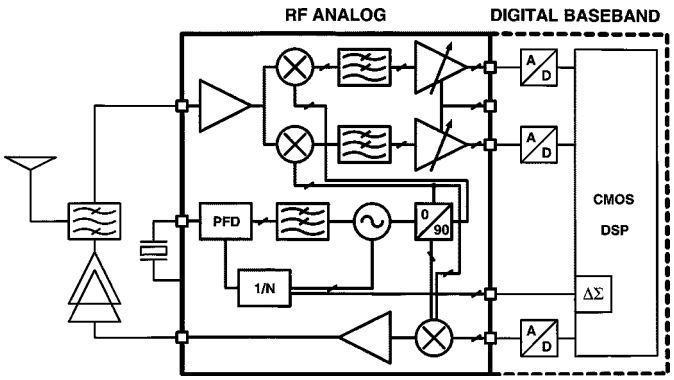

Fig. 1. CMOS transceiver system. The bold box indicates the integrated front-end.

II. RX Architectures

The most popular way to implement RXs is the super-heterodyne architecture. It combines subsequent down-conversion stages with high-Q interstage filtering. The accuracy of the mirror signal suppression does not rely on matching local oscillator (LO) feedthrough and dc offsets (systematic and dynamic) do not affect the signal quality. The signal that needs to be processed is bandpass filtered and limited in dynamic range (DR) by the high-Q filters, resulting in relaxed specification of all building blocks, including the analog-to-digital (AD) converters. However, the high-Q filters come at the cost of area (i.e., money) and they have a parasitic effect on the power consumption. Due to the insertion loss, more gain is needed to achieve the SNR. Furthermore, to interface the low-impedance level of the filters (e.g., 50 Ω) impedance transformation—with high-quality integrated passives—or low-output impedance buffering is needed, which has a negative effect on the power budget.

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Since CMOS implementation is only justified when it can provide a cheaper solution than its BiCMOS/bipolar counterpart, RX architectures with a higher integrability, such as zero-IF [4] and low-IF RXs [5], which are preferred topologies (see Fig. 1). Both architectures feature single-stage dual path quadrature down-conversion without high Q filters. The number of external nodes is minimized, increasing the robustness of the front-end and decreasing the sensitivity to interference and crosstalk. The architecture also fully exploits the core competence of CMOS by assigning the image rejection, channel selection, and demodulation to the digital domain. The bottleneck of zero-IF RXs is $1/f$ noise and mismatch-related or self-mixing related offsets that corrupt the wanted signal at low frequencies. To compensate the offsets, sophisticated feedback through the digital signal processor (DSP) can be implemented, but due to the finite time constant of the loop, part of the wanted signal will also be attenuated. The low-IF RX alleviates this problem by setting the IF frequency to typically one-half the channel bandwidth [5]. Saturation of the AD by dc offsets is avoided by adding 1/2 bit to the AD DR. The necessary image-rejection ratio (IMRR) spec for cellular applications is 32 dB, which is easily manageable in CMOS (i.e., $\Delta\phi \approx 2^\circ$ and $\Delta A \approx 0.3$ dB). The IMRR specification for the low-IF RX is set by the adjacent channel interference owing to the channel at 400-kHz offset from the wanted signal. The tail of this adjacent channel directly interferes with the wanted signal after down-conversion at 200 kHz. Since this interferer can be 41 dB higher than the wanted signal (ETSI GSM 05.05 v. 5.4.1) and acts as an adjacent channel at 200 kHz, which can be 9 dB higher than the wanted signal, while preserving the bit error rate (BER), the needed IMRR is 32 dB. For full integration of high-end RF systems, the low-IF topology seems the best solution. This becomes clear in several recently published RF-CMOS circuits in the area of GPS [17] or Bluetooth applications [18]–[20].

III. Low-Power CMOS Low-Noise Amplifiers

The low-noise amplifier (LNA) design incorporates in a single transistor the main front-end design tradeoffs: impedance matching, power, linearity, noise and bandwidth. LNAs with a common-gate input gate, though convenient for providing a good 50-Ω match, provide an inherently too high noise figure (NF). Therefore, the LNA topology (Fig. 2) discussed here employs an input-matched cascode topology with inductive source degeneration. Since the required S_{11} is typically only -10 dB (Table I), an extra degree of freedom can be introduced by realizing a nonperfect input match. The available power of the source is by definition given by (1)

$$P_{\text{av}} = \frac{v_{\text{eq}}^2}{4R_{\text{eq}}} = \frac{v_s^2}{4R_s} \tag{1}$$

where $R_s = 50\ \Omega$. The output power of the LNA is determined by the equivalent load resistance (R_{load}) of the LNA and by the current injected in that load (2)

$$P_{\text{out}} = i_{\text{out}}^2 R_{\text{load}}. \tag{2}$$

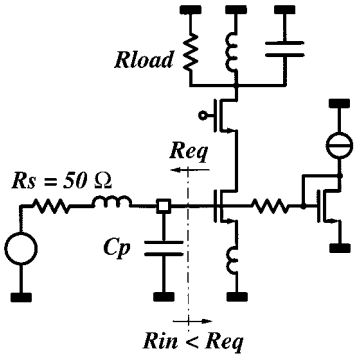

Fig. 2. Input matched cascode LNA circuit.

TABLE I
Building-Block Specifications

Specification	TRX	DCS-1800
Low-IF RX		
NF	6.2 dB	8.9 dB
IMRR	32.2 dB	32 dB
Gain	54.5 dB	−−
S11	<-11.5 dB	-10 dB
IIP3	>-6.2 dBm	-23.5 dBm
LO Leakage	<-63 dBm	-47 dBm
Power	113 mW	ALAP
4th order, type-II PLL		
Settling	226 μs	288 μs
PN @ 600 kHz	-125 dBc/Hz	- 116 dBc/Hz
PN @ 3 MHz	-144 dBc/Hz	- 133 dBc/Hz
$\Delta\Phi_{RMS}$	1.7°	2°
Spurs	-84 dBc	-80 dBc
Power	70 mW	ALAP
Direct Upconversion TX		
Output Power	-13 dBm	0 dBm
Mirror Suppr.	-33 dBc	-30 dBc
LO Feedthr.	-38 dBc	-30 dBc
GMSK Mask	Compliant	ETSI
Power	82 mW	ALAP

R_{load} mainly consists of the equivalent parallel resistance of the load inductor. The inductance itself is tuned out by the excess capacitance at that node. The output current i_{out}^2 is given by

$$i_{\text{out}}^2 = i_{\text{in}}^2 \left(\frac{\omega_T}{\omega_0}\right)^2 \tag{3}$$

where

$$i_{\text{in}}^2 = \frac{4P_{\text{av}}R_{\text{eq}}}{(R_{\text{eq}}+R_{\text{in}})^2}. \tag{4}$$

From (1)–(4), it is seen that the highest level of power gain for a given frequency and value of ω_T is obtained by making the input impedance R_{in} as low as possible. This means that even though less power is absorbed at the input of the LNA, the power is used more efficiently to generate output current and, hence, output power. It is further seen that the power gain of the LNA increases with increasing ω_T, i.e., with deeper submicrometer CMOS technology or with increasing $V_{\text{GS}}-V_T$. Note that, for input matching (it is important to include the nonquasi-static (NQS) effect), a phase lag in the channel charge built up. Although it is an inherently HF (≈100 GHz) effect, due to the resonance at the LNA input, the NQS is seen as an extra gate resistance (5) [6], [7]

$$R_{G,\,\text{NQS}} = \frac{1}{\kappa g_{d0}}, \qquad \kappa = 5. \tag{5}$$

This implies that R_{in} can never be set lower than $R_{G,\,\text{NQS}}$ (around 20 Ω).

Noise considerations are also best done on the reference plane of R_{eq} (see Fig. 2). The NQS effect should be taken into account in the noise analysis. It implies a time-variant channel charge, resulting in an equivalent input noise current, yielding the following approximate expression for the NF of the LNA [6], [7]

$$\text{NF} \simeq 1 + \underbrace{\left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\gamma}{\alpha} g_m R_{\text{eq}}}_{\text{Classic Noise}} + \underbrace{\left(\frac{\omega_0}{\omega_T}\right)^2 \frac{\gamma}{\alpha}\frac{2}{\kappa} + \frac{\alpha\delta}{\kappa g_m R_{\text{eq}}}}_{\text{NQS Noise}} \tag{6}$$

with α, γ, and δ are known transistor parameters. R_{eq} represents the equivalent source resistance, which is seen at the gate of the input transistor. The value of R_{eq} is determined by the parasitic capacitance C_p, which is always present at the input of the LNA. Part of this capacitance stems from the input bonding pad and from a possible input electrostatic discharge (ESD)-protection network. A higher C_p will cause a higher value for R_{eq}. For high R_{eq}, the noise is determined by classic noise, but at low R_{eq}, the NF increases again due to the NQS noise. Based on (1)–(6), it is seen that the NF decreases and the power gain increases with increasing ω_T. As such, deeper submicrometer technologies automatically improve both NF and gain of the LNA.

Another issue to be considered when designing a CMOS LNA is its sensitivity to ESD at the input. The presence of the gate oxide drastically increases the susceptibility to electrical overstress. As technologies progressively scale down, so does the oxide thickness, which makes matters even worse. A tradeoff between RF performance and ESD immunity should be made.

The LNA presented in [2] has been designed as a standalone 50-Ω-in 50-Ω-out LNA to be used in an $L2$-band GPS RX. The circuit is equipped with an on-chip ESD-protection network. The LNA uses basically the same topology that has been discussed above. The input bonding pad consists of only the top metal layer in order to reduce its capacitance. The grounded bottom metal layer increases the Q of the pad, decreasing its noise contribution and isolating the input from the substrate. Two reverse-biased diodes protect the input of the LNA against ESD pulses. Their capacitance adds to the capacitance of the bonding pad. Together they constitute the major part of the input capacitance C_p discussed earlier.

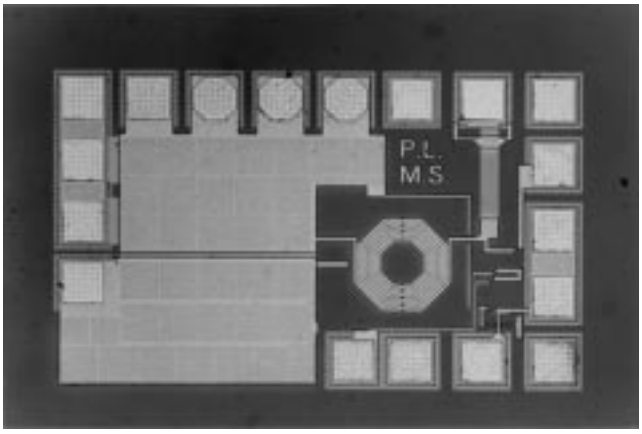

Fig. 3. 0.8-dB NF 0.25-μm CMOS LNA.

The LNA, operating at 1.24 GHz, draws 6 mA from a 1.5-V supply, yielding a total power consumption of merely 9 mW. The input and output reflection coefficients are −11 dB. The power gain of the LNA is 20 dB, while the reverse isolation ($-S_{12}$) is more than 30 dB. The LNA features a very low NF of 0.8 dB. The input referred third-order intermodulation intercept point (IIP3) of the circuit is −11 dBm, which is more than sufficient for the GPS application. A human body model (HBM) test has shown that the input of the LNA is able to withstand pulse from −1.4 to 0.6 kV. The chip micrograph is shown in Fig. 3.

IV. Quadrature Down-Conversion Mixers

Since MOS transistors have a much higher IIP3 than bipolar transistors, it is possible to integrate "linear" mixers. Therefore, more gain can be assigned to the LNA, relaxing the noise specs of the mixers. To achieve comparable linearity in bipolar mixers, emitter degeneration is necessary, neutralizing the bipolar power advantage and increasing the NF. In the circuit topology of Fig. 4, the down-conversion mixer employs a cascoded current-folding switching mixer topology. The folding allows 2-V operation while enabling the insertion of a cascode transistor $M2$ to reduce LO leakage and LO self-mixing. The cascode transistor, together with a large $V_{\text{GS}}-V_T$ for $M1$ sets the mixer IIP3 to +17 dBm.

The white noise contribution to the NF is mainly determined by the limited $V_{\text{GS}}-V_T$ of the top current source $M4$. By adding a PMOS bleeder $M3$, biased at a much higher $V_{\text{GS}}-V_T$ than $M4$, the total noise for the same current can be decreased. The total white NF of the RX is 3.9 dB. Due to the low-IF architecture, the NF is corrupted by residual $1/f$ noise injected by incomplete switching. Therefore, the area of $M5$ and $M6$ should be maximized. The total $1/f$ NF is 2.4 dB. With a total NF of 6.2 dB, signals as low as −100 dBm can be detected with an SNR of 11 dB (DCS1800 and GSM applications).

The pole on the switching node sets the efficiency/speed limitation of the mixer. The addition of $M2$ and $M3$ gives an extra

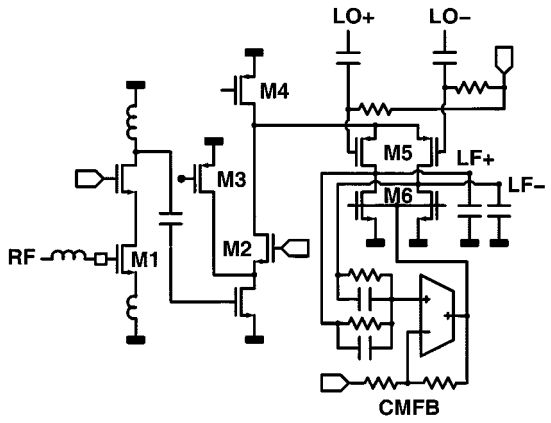

Fig. 4. LNA and the (I/Q) down-conversion mixers.

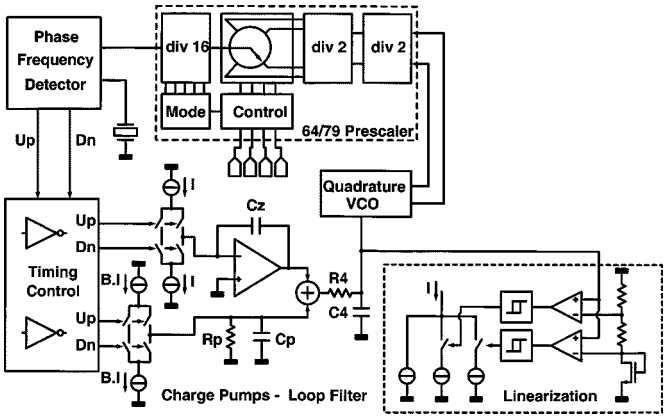

Fig. 5. Fourth-order type-II dual-path PLL.

degree of freedom to obtain higher pole frequencies. In principle, the current through $M2$ can be lowered until the pole on the cascode node is degraded. In practice, the minimum current is set by the maximum input signal of the mixer: $I_{2,\min} > g_{m1} v_{in,\max}$. Other considerations that set the sizes of the mixer transistors are input loading of the PLL and dc offset.

V. Phase-Locked-Loop Circuits

To fully integrate the phase-locked loop (PLL) frequency synthesizer in CMOS, phase noise and spurious suppression must be traded off against integrated capacitance (i.e., area) and settling time. Again, there is no substitute for cubic inches since large external capacitors can implement the large time constant of the loop filter without large resistors (i.e., noise). Not only a 64/79 prescaler, a zero-dead-zone phase-frequency detector (PFD), charge pumps, and a three-step equalizer are integrated, but also the quadrature *LC*-tank voltage-controlled oscillator (VCO), as well as a third-order 35-kHz low-pass loop filter, reducing transmitted signal pickup and area. To achieve this level of integration, a dual-path filter topology has been implemented (Fig. 5). Two filter paths [one integration (C_z) and one low-pass filter (C_p, R_p)] are added to reveal the zero needed for loop stability in a type-II PLL without additional capacitance [8]. The number of capacitors is the same as in a classical fourth-order type-II PLL, but for the same phase noise, the integrated capacitance is more than five times smaller (only 1.4 nF).

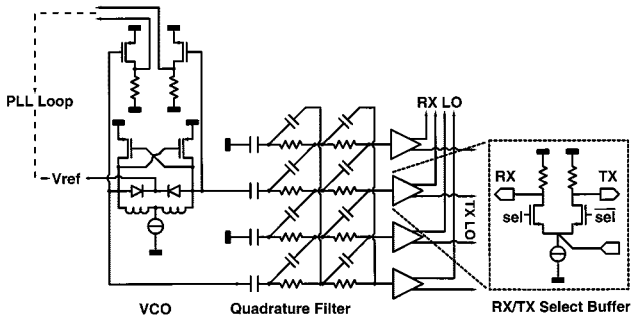

Fig. 6. PMOS VCO circuit with direct polyphase loading and output buffers.

The out-of-band phase noise of a PLL is mainly determined by the VCO (see Section VI). The in-band phase noise, however, is determined by the remaining loop components and is multiplied by the division factor of the prescaler. To achieve a fine frequency resolution, a high division factor is needed, severely deteriorating the in-band noise and, consequently, the rms phase error $\Delta\Phi_{\mathrm{RMS}}$, which may not exceed 2°, i.e., -80 dBc/Hz in a 35-kHz band. By using delta–sigma fractional-N techniques [9], a higher reference frequency can be chosen (26 MHz), lowering the division factor (i.e., in-band noise) and enabling faster settling (i.e., higher loop bandwidth). The drawback of this technique is spur generation at fractional multiples of the reference frequency. Even by increasing the order of the $\Delta\Sigma$ modulator or by adding dithering, the spurs cannot totally by neutralized because of substrate and power supply line coupling. Additionally, mixing by nonlinearities (e.g., a small dead zone) in the PFD results in reappearance of randomized spurs and in-band noise leakage. The implementation of the $\Delta\Sigma$ modulator is assigned to the DSP (Fig. 1).

The main contributors to the PLL power consumption are the prescaler (9 mW) and the VCO (46 mW). Since the prescaler is, in fact, a digital circuit, its power will go down with scaling technology. The VCO power consumption, however, relies on the integration of high-Q passives.

VI. VCO

For high-end applications, *LC*-tank oscillators are the best choice. Their power consumption, as well as their phase noise, depends on the quality of the integrated passives shown in the following equation, one of the major weaknesses of standard CMOS technology [8]:

$$\mathcal{L}(\triangle\omega) = kT \cdot R_{\mathrm{eff}} \cdot (1+A) \left(\frac{\triangle\omega}{\omega_0}\right)^2 \frac{2}{A_{\mathrm{diff}}^2} \qquad (7)$$

with R_{eff} being the effective tank resistance, A being the excess gain, and A_{diff} being the differential amplitude of oscillation. R_{eff} is mainly determined by the integrated inductor. A simulator-optimizer program has been developed [3], which yields an optimal set of inductor geometry parameters for a certain technology. The result is an inductor with a Q of nine, integrated in standard 0.25-μm CMOS with only two metal layers ($M1$: 0.6 μm, $M2$: 1.0 μm) and a moderate substrate resistance of 5 $\Omega \cdot$ cm.

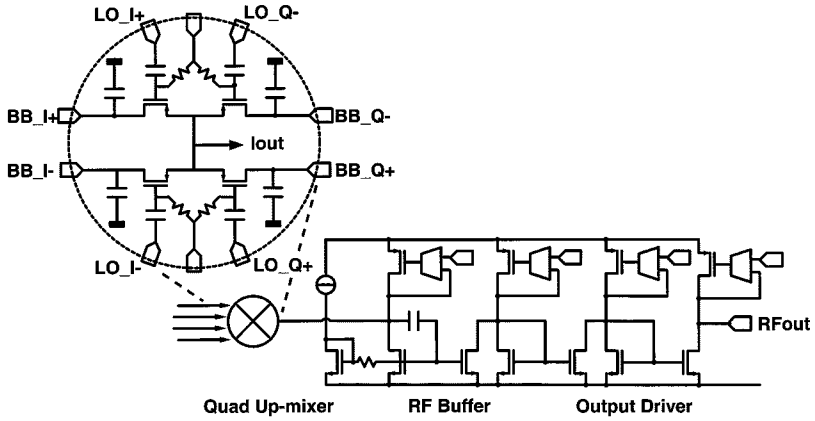

Fig. 7. I/Q up-converter mixers and preamplifier.

Due to intensive research, the Q of integrated inductors is improving, such that the varactor Q can become an issue. MOS transistors used as varactors achieve wide, but highly nonlinear tuning characteristics. Also, the Q is low at its minimum (≈10) and varies seriously with tuning voltage. However, for deep submicrometer CMOS, the MOS capacitors Q increases due to smaller channel length L as shown in the following:

$$Q_{MOS} \sim \frac{\mu(V_{\rm GS} - V_T)}{\omega L^2}. \tag{8}$$

More commonly, p+/n diode varactors are used. By optimized symmetrical layout, a linear tuning range and a Q of around 45 can be achieved. The diode varactor limits the VCO gain, which is beneficiary for noise and PLL stability, but limits the tuning range. By using a PMOS VCO topology (Fig. 6), the full voltage range (0–Vdd) can be exploited to tune, resulting in 28% tuning range for 1.8 V. Furthermore, the diodes never reach forward bias condition, such that the phase noise degrades very little over tuning range.

Last but not least, up-conversion of white and $1/f$ noise of the active devices can be minimized. In (7), A is 2.5–3.5, which means that, by transistor noise reduction, more than 6 dB in phase noise can be gained. Noise up-conversion is related to oscillation symmetry [10]. In [11], $1/f$ noise up-conversion is minimized by proper choice of the VCO biasing and by making an ideal ac ground at the current source drain. Further reduction of noise up-conversion can be achieved by impeding the conversion of noise currents in output voltage noise [12].

VII. Quadrature Generation

Quadrature signal generation can be performed with a master–slave flip-flop in combination with a VCO at 2× the required frequency. However, this approach is very power hungry and very sensitive to process variations in the prescalers. For that reason, polyphase filter (PF) approaches have been introduced [5]. A second-order PF can provide an I–Q accuracy of over 35 dB over several hundreds of megahertz, ensuring the operation bandwidth over process tolerances. Higher order PFs result in a better accuracy and a larger frequency band, but at the cost of higher power in the buffers. Although the passive *RC* filter does not consume any dc power, the VCO–polyphase interface buffers are very power hungry. In this design, the VCO drives the PF directly (Fig. 6). In buffered PF design, the resistors are small (≈30 Ω) [13] to reduce signal loss. In the directly driven case, these low real impedance levels have a detrimental effect on the phase noise. However, by omitting the input buffers, a larger signal can be applied at the PF input, enabling lower power consumption in the output buffer (1 mA) and higher resistor values. Also, by lowering the capacitive load of the mixer, the resistor values can be increased. However, the size decrease of the mixer transistors is limited by the necessary mixer gain, the gain in the preamplifers, and matching performance. The total resistance of the PF is 500 Ω, which is mainly concentrated in the resistor closest to the VCO, deteriorating the VCO phase noise with only 1.8 dB (Table I). The choice of the coupling capacitor between the VCO and the PF also imposes a tradeoff between signal loss and phase noise. An optimal value of 2 pF is chosen.

The quadrature oscillator, mixers, and preamplifiers have been optimized as one building block, trading off signal loss and VCO phase noise against global power consumption. The resulting power reduction in the PF is almost 70 mW.

VIII. CMOS Up-Converter Circuits

For up-conversion, a direct up-conversion topology is again in favor toward higher integration. Image canceling is performed by balanced double quadrature up-conversion instead of high Q external filters. Since in CMOS, Gilbert-type up-conversion mixers result in high LO feedthrough and high power and noise to lower the distortion, a transconductance mixer with four NMOS transistors biased in their linear region is developed (Fig. 7). The mixer converts the BB and LO signals into a linear RF modulated current as follows:

$$I_{\rm mixer} = \delta \cdot \mu C_{ox} \frac{W}{L} \left(v_{bb,I}^2 + v_{bb,Q}^2 + 2 v_{lo} v_{bb} \right). \tag{9}$$

δ models the degeneration of the modulated current due to a nonideal virtual ground at the mixer RF output and the BB inputs. The modulated current is converted to a voltage by the finite conductance. A low-frequency (LF) loop (OTA and PMOS in Fig. 7) provides a low impedance (<1 Ω) at low frequencies, thereby minimizing intermodulation products. A HF loop

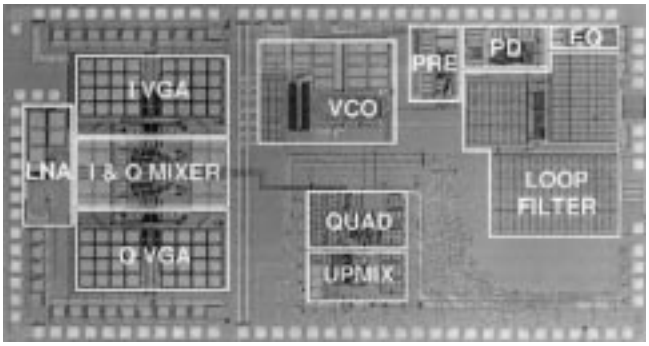

Fig. 8. Microphotograph of the fully integrated CMOS transceiver front-end.

(capacitive drain–gate connected NMOS) prevents degeneration of the RF signal and mirrors the RF signal to the next stage. The ac coupling also enables low-voltage operation. At the BB nodes, large capacitors conduct the modulated RF currents to ground and not through the bonding wires, making the RF signal linearity and amplitude independent of the bonding wire's matching and length

$$HD3 = \frac{1}{32} \cdot \frac{\triangle V_T}{V_{\rm GS} - V_T} \left(\frac{I_{\rm ac}}{I_{\rm DC}} \right)^2. \tag{10}$$

Current folding in the RF buffer and output driver (Fig. 7) ensures good linearity with low dc currents. The large transistor width (for high currents) results in good matching and, thus, low $\triangle V_T$. Hence a low $I_{\rm DC}/I_{\rm ac}$ is possible while maintaining low distortion specifications (10). By making all NMOS drain–source voltages equal and by adding LF feedback loops, an optimal linear behavior is achieved.

To minimize LO feedthrough, "cold" mixers are implemented, meaning that the drain–source voltage of the mixer transistors is zero to prevent mixing with the LO signal. However, due to mismatch in the mixer transistors, capacitive LO feedthrough is not fully cancelled at the virtual ground nodes. Since the transistor matching is limited by the capacitive loading of the PF (see Section VII), the resulting LO feedthrough is around -38 dBc (Table I). Fig. 8 shows the microphotograph of the 2-V fully integrated transceiver front-end implemented in 0.25-μm standard CMOS technology.

IX. CMOS Power Amplifiers

Today's power amplifiers are implemented in GaAs, heterojunction bipolar transistors (HBTs), LDMOS, and BiCMOS using conventional biasing schemes. However, more and more signal processing is done in CMOS. For this reason, a single-chip transceiver demands an integrated CMOS power amplifier. In CMOS, switching mode power amplifiers are the favored candidates for wireless communications due to their excellent efficiency. Most CMOS power amplifiers that are being published use differential class-E output signals [14]–[16]. Substrate coupling is solved because there is less injection of common mode noise in to the substrate. The current is discharged to ground twice per cycle, reducing interference with the desired signals. However, the biggest

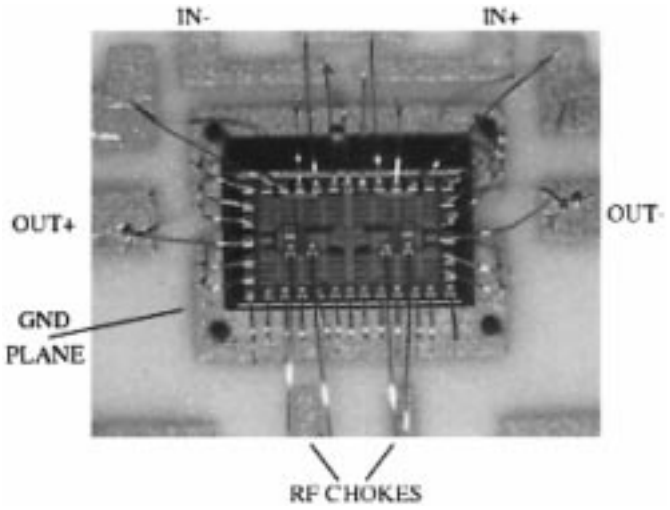

Fig. 9. 1-W 62% PAE CMOS power amplifier.

benefit is undoubtedly gain boosting. The voltage at the drain of the class-E amplifier is swept up to approximately 3.6 times the supply voltage. In a differential structure, this voltage can be positively fed back, reducing the size of the NMOS transistors. The power amplifier must be designed for handling large currents. This results in a larger silicon area because larger transistors and wider traces are required. Increasing the switch transistors has the benefit of reducing the on resistance, but the penalty, of course, is that a smaller inductor needs to be used to tune out the gate capacitance. Aluminum bonding wires are being used as inductors because any parasitic resistance of the inductor reduces the efficiency drastically. An example of a high-efficiency 700-MHz 1-W CMOS power amplifier realized in a 0.35-μm CMOS (5M2P) technology is shown in Fig. 9 [14]. The total chip area is 2.64 mm^2. Special care has been taken to comply with the electromagnetic rules and to obtain maximum symmetry. The outputs are placed at opposite sites of the die, which reduces the coupling between the inductors. The power amplifier is capable of transmitting a 1-W Gaussian mimimum shift-keying (GMSK) spectrum, with a power-added efficiency (PAE) of 62%, which is, up to date, one of the highest reported CMOS realizations.

X. Conclusions

An overview of the use of CMOS for low-cost integration of a high-end cellular RF transceiver front-end has been presented. The fundamental pitfalls and limitations of RF CMOS have been discussed. These obstacles have been circumvented through the choice of transceiver architecture, circuit topology design, and systematic optimization of the different transceiver blocks. Optimization of the transceiver as one single block by minimizing the number of power-hungry interface circuits has been emphasized. As examples, a fully integrated 2-V CMOS cellular transceiver front-end has been demonstrated. Further more, a low-power 0.8-dB NF CMOS low-noise amplifier and a highly efficient power amplifier have been discussed, highlighting the general applicability of CMOS for low-power RF transceivers.

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